60V 4-Switch Buck-Boost Controller

DESCRIPTION

The VE8624 is a synchronous 4-switch buck-boost voltage/current regulator controller. The VE8624 can regulate output voltage, output current, or input current with input voltages above, below, or equal to the output voltage. The constant-frequency, current mode architecture allows its frequency to be adjusted from 100kHz to 700kHz. No top FET refresh switching cycle is needed in buck or boost operation. With 60V input, 60V output capability and seamless transitions between operating regions, the VE8624 is ideal for voltage regulator, battery/super-capacitor charger applications in automotive, industrial, telecom, and even battery-powered systems.

The VE8624 provides input current or output current monitor, and various status flags, such as C/10 charge termination output flag.

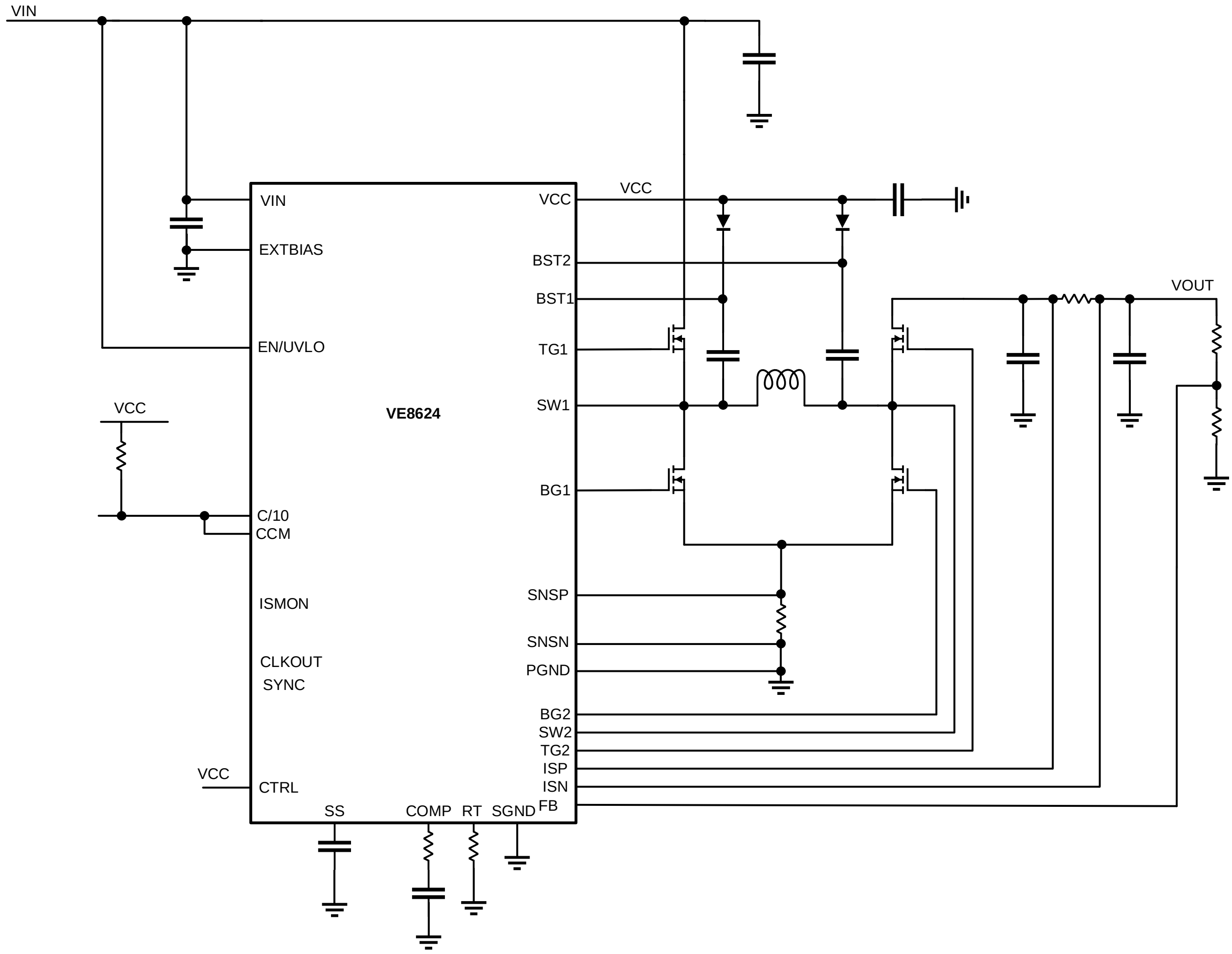
FEATURES

- 4-Switch Single Inductor Architecture Allows VIN Above, Below or Equal to VOUT
- Synchronous Switching: Up to 98.5% Efficiency
- Wide VIN Range: 4.7V to 60V
- 2% Output Voltage Accuracy:
  $1.2V \le V_{OUT} \le 60V$
- 6% Output Current Accuracy:
  $3V \le V_{OUT} \le 60V$
- Input or Output Current Regulation with Current Monitor Outputs
- No Top FET Refresh in Buck or Boost
- VOUT Disconnected from VIN During Shutdown
- C/10 Charge Termination
- Easy Parallel Capability to Extend Output Power
- Available in 28-Lead TSSOP with Exposed Pad

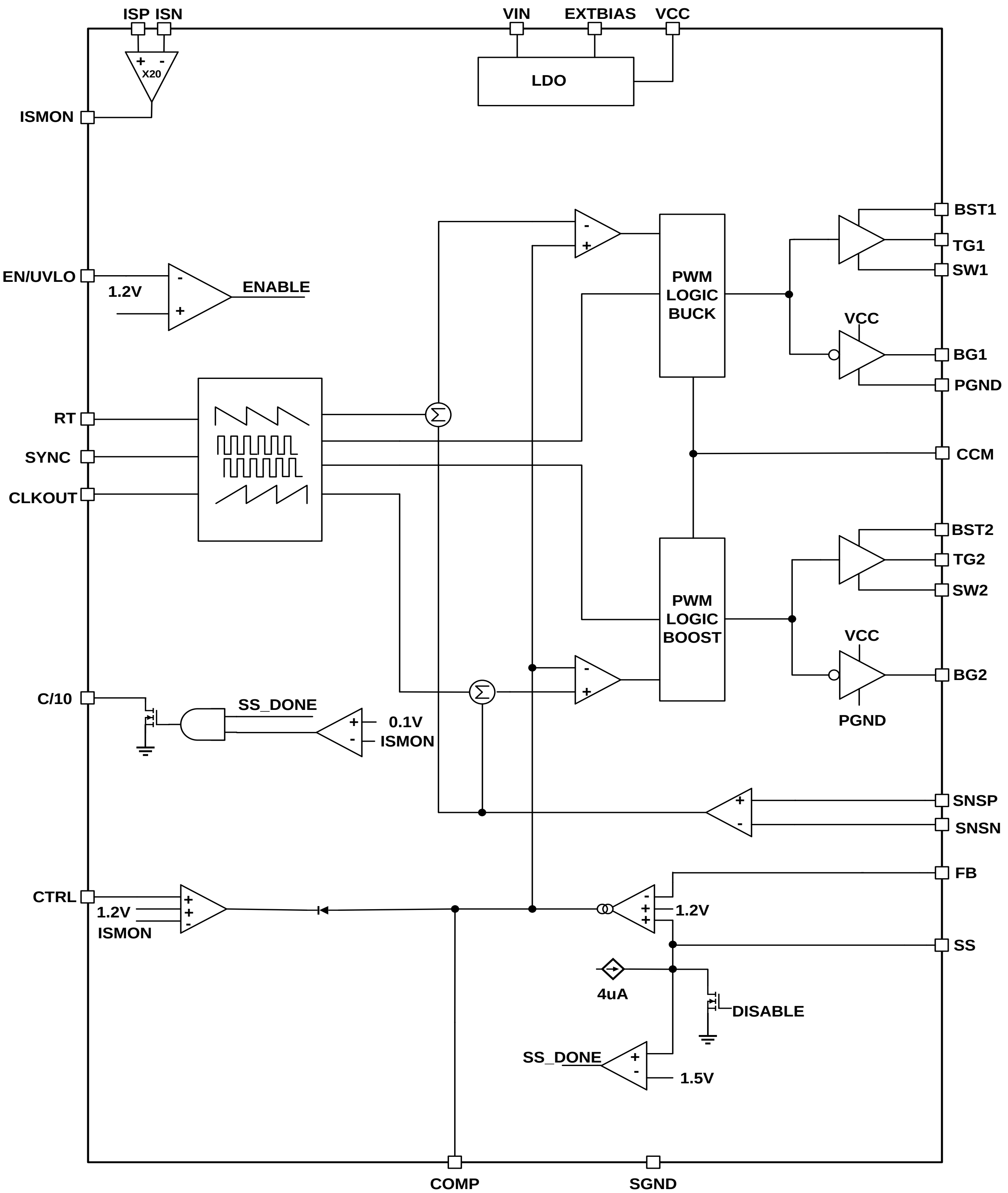
APPLICATIONS

- Automotive, Telecom, Industrial Systems
- High Power Battery

TYPICAL APPLICATION

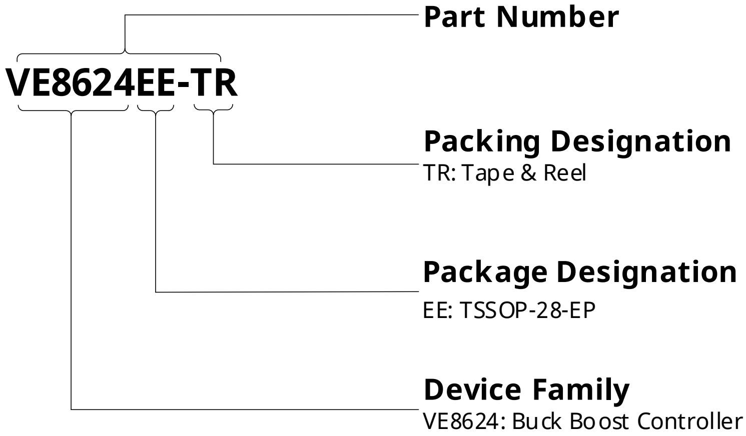


BLOCK DIAGRAM

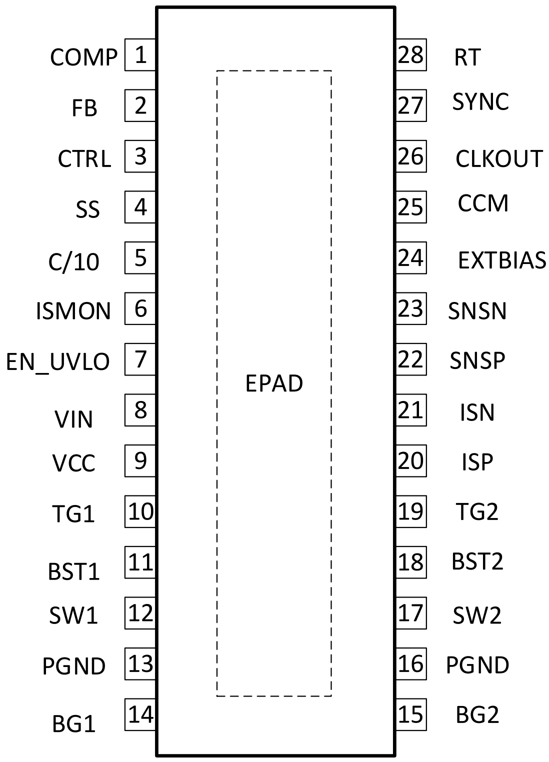


ORDERING INFORMATION

Ordering Information	Mark	Temperature Range	Package	Pack	Quantity
VE8624EE-TR	8624	-40 to +125°C	TSSOP-28-EP	TR	4000



PIN CONFIGURATIONS



TSSOP28-EP

PIN DESCRIPTION

Pin	Name	Description
1	COMP	Current Control Threshold and Error Amplifier Compensation Point.
2	FB	Voltage Loop Feedback Pin. FB is intended for constant-voltage regulation. The internal transconductance amplifier with output VC will regulate FB to 1.2V (typical) through the DC/DC converter.
3	CTRL	Output Current Sense Threshold Adjustment Pin. Regulating threshold $V_{(ISP-ISN)}$ is 1/20th of V_{CTRL}. CTRL linear range is from 0V to 1.1V. For V_{CTRL} > 1.4V, the current sense threshold is constant at the full-scale value of 60mV. For 1.1V < V_{CTRL} < 1.4V, the dependence of the current sense threshold upon V_{CTRL} transitions from a linear function to a constant value, reaching 98% of full scale by V_{CTRL} = 1.2V. Connect CTRL to VREF for the 60mV default threshold. Force less than 50mV (typical) to stop switching. Do not leave this pin open.
4	SS	A regulated 4uA current charges up the SS capacitor. The value of this SS capacitor sets the output voltage ramp.
5	C/10	C/10 Charge Termination Pin. An open-drain pull-down on C/10 asserts if $V_{(ISMON)}$ is less than 100mV (typical). To function, the pin requires an external pull-up resistor.
6	ISMON	Monitor pin that produces a voltage that is twenty times the voltage $V_{(ISP-ISN)}$. ISMON will equal 1.2V when $V_{(ISP-ISN)}$ = 60mV. For parallel applications, tie master VE8624 ISMON pin to slave VE8624 CTRL pin.
7	EN/UVLO	Enable Control Pin. Forcing an accurate 1.2V falling threshold with 125mV hysteresis. An undervoltage condition resets soft-start. Tie to 0.3V, or less, to disable the device and reduce VIN quiescent current below 1µA.
8	VIN	Main Input Supply. Bypass this pin to PGND with a capacitor.
9	VCC	Internal 5V Regulator Output. The driver and control circuits are powered from this voltage. Bypass this pin to PGND with a minimum 4.7µF ceramic capacitor.
10	TG1	Top Gate Drive. Drives the top N-channel MOSFET with a voltage equal to V_{CC} superimposed on the switch node voltage SW1.
11	BST1	Bootstrapped Driver Supply. The BST1 pin swings from a diode voltage below V_{CC} up to a diode voltage below V_{IN} + V_{CC}.
12	SW1	Switch Node. SW1 pin swings from a diode voltage drop below ground up to VIN.
13,16	PGND	Power Ground. Connect these pins closely to the source of the bottom N-channel MOSFET.
14	BG1	Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and V_{CC}.
15	BG2	Bottom Gate Drive. Drives the gate of the bottom N-channel MOSFET between ground and V_{CC}.
17	SW2	Switch Node. SW2 pin swings from a diode voltage drop below ground up to V_{OUT}.
18	BST2	Bootstrapped Driver Supply. The BST2 pin swings from a diode voltage below

Pin	Name	Description
		V_{CC} up to a diode voltage below V_{OUT} + V_{CC}.
19	TG2	Top Gate Drive. Drives the top N-channel MOSFET with a voltage equal to V_{CC} superimposed on the switch node voltage SW2.
20	ISP	Connection Point for the Positive Terminal of the Output Current Feedback Resistor. Input bias current for this pin is typically 270µA.
21	ISN	Connection Point for the Negative Terminal of the Output Current Feedback Resistor.
22	SNSP	The Positive Input to the Current Sense Comparator.
23	SNSN	The Negative Input to the Current Sense Comparator.
24	EXTBIAS	External bias input for the optional VDD LDO. There is an internal switch to disconnect the VIN LDO when EXTBIAS voltage is higher than 4.7V. Decouple this pin to ground with a 4.7µF ceramic capacitor when it is in use. Connect to GND if it is not used.
25	CCM	Continuous Conduction Mode Pin. When the pin voltage is higher than 1.5V, the part runs in fixed frequency forced continuous conduction mode and allows the inductor current to flow negative. When the pin voltage is less than 0.3V, the part runs in discontinuous conduction mode and does not allow the inductor current to flow backward. This pin is only meant to block inductor reverse current, and should only be pulled low when the output current is low. This pin must be either connected to V_{CC} for continuous conduction mode across all loads, or it must be connected to the C/10 with a pull-up resistor to V_{CC} for continuous conduction mode at heavy load and for discontinuous conduction mode at light load.
26	CLKOUT	Clock Output Pin. A 180° out-of-phase clock is provided at the oscillator frequency to allow for paralleling two devices for extending output power capability.
27	SYNC	External Synchronization Input Pin. The internal buck clock is synchronized to the rising edge of the SYNC signal while the internal boost clock is 180° phase shifted.
28	RT	Frequency Set Pin. Place a resistor to GND to set the internal frequency. The range of oscillation is 100kHz to 700kHz.
29	EPAD	Signal Ground. Solder the exposed pad directly to the ground plane.

ABSOLUTE MAXIMUM RATINGS

Parameter	Minimum	Maximum	Unit
PVIN, SVIN	-0.3	+75	V
EXTBIAS	-0.3	+30	
SW1, SW2	-0.3(-5V 20ns)	+75	V
C/10	-0.3	+15	V
EN/UVLO, ISP, ISN	-0.3	+75	V
VCC, BST1-SW1, BST2-SW2	-0.3	+6.5	V
ISP-ISN, SNSP-SNSN	-0.3	+0.3	V
SNSP, SNSN	-0.3	+0.3	V
Other Pins	-0.3	+6.5	V
Storage Temperature	-65	+150	°C

ESD RATINGS

Parameter	Value	Unit
Human Body Model (HBM), per AEC-Q100-002		kV
Charged Device Model (CDM), per AEC-Q100-011		kV
Latch-Up, per AEC-Q100-004		mA

THERMAL INFORMATION

Thermal Resistance	θ_{JA}(°C/W)	θ_{JC}(°C/W)
TSSOP28-EP	40	8

RECOMMENDED OPERATINIG CONDITIONS

Parameter	Minimum	Maximum	Unit
VIN	+4.7	+60	V
EXTBIAS	+4.7	+24	V
VOUT	+1.2	+60	V
Operating Junction Temperature	-40	+125	°C

ECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the specified operating junction temperature range, otherwise specifications are at T_A = 25°C (Note 2). V_{IN} = 12V, unless otherwise noted.

Parameter	Symbol	Condition		Min	Typ	Max	Unit
Input Supply							
V_{IN} Operating Voltage	V_{IN}		●	4.5		60	V
V_{IN} Shutdown I_Q	I_{shut}	$V_{EN/UVLO}$ = 0V			2		µA
V_{IN} Operating I_Q (Not Switching)	I_Q	FB = 1.3V, RT = 90k			3.0		mA
Logic Inputs							
EN/UVLO Rising Threshold	V_{EN}		●		1.2		V
EN/UVLO Hysteresis			●		120		mV
EN/UVLO Pin Bias Current High		$V_{EN/UVLO}$ = 2V			1		uA
CCM Threshold Voltage				0.3		1.5	V
Regulation							
V(ISP-ISN) Threshold		V_{CTRL} = 2V, V_{ISP} = 12V	●		60		mV
		V_{CTRL} = 2V, V_{ISP} = 1V			60		mV
		V_{CTRL} = 1V, V_{ISP} = 12V	●		50		mV
		V_{CTRL} = 1V, V_{ISP} = 1V			50		mV
		V_{CTRL} = 0.6V, V_{ISP} = 12V	●		30		mV
		V_{CTRL} = 0.6V, V_{ISP} = 1V			30		mV
		V_{CTRL} = 0.1V, V_{ISP} = 12V	●		5		mV
		V_{CTRL} = 0.1V, V_{ISP} = 1V			5		mV
ISP Bias Current	I_{ISP}	V_{ISP} = 12V, V_{ISN} = 12V			270		µA
ISN Bias Current	I_{ISN}	V_{ISP} = 12V, V_{ISN} = 12V				1	µA
Output Current Sense Common Mode Range	$V_{SENSE+/-}$			0		60	V
Output Current Sense Amplifier gm					250		µS
ISMON Monitor Voltage	V_{ISMON}	$V_{(ISP-ISN)}$ = 60mV	●		1.2		V
FB Regulation Voltage	V_{FB}		●		1.2		V
FB Amplifier gm					500		µS
FB Pin Input Bias Current	I_{FB}	FB in Regulation				100	nA
COMP Standby Input Bias Current	I_{COMP}	PWM = 0V		-20		20	nA
VSENSE(MAX) (VSNSP-SNSN)		Boost	●	46	55	60	mV
		Buck	●	-50	-40	-30	mV

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Fault						
SS Pull-Up Current	I_{SS}	V_{SS} = 0V		4		μA
C/10 Falling Threshold (V_{ISMON})		VFB = 1.2V		100		mV
C/10 Pin Output Impedance				0.2		kΩ
SS Reset Threshold				0.2		V
Oscillator						
Switching Frequency	F_{SW}	RT =90k		500		kHz
	F_{SWH}	MAX	700			kHz
	F_{SWL}	MIN			100	kHz
SYNC Frequency	F_{SYNC}		150		400	kHz
SYNC Pin Resistance to GND	R_{SYNC}			200		kΩ
SYNC Threshold Voltage	F_{SYNC_TH}		0.3		1.5	V
Internal V_{CC} Regulator						
VCC Regulation Voltage			4.8	5	5.2	V
Dropout (VIN – VCC)		I_{VCC} = 10mA, V_{IN} = 5V		240	350	mV
V_{CC} Undervoltage Lockout			3.1	3.5	3.9	V
V_{CC} Current Limit	$ILIMIT_{\_VCC}$	V_{CC} = 4V		67		mA
VCC from EXTBIAS Regulation Voltage	$VCC_{EXTBIAS}$			5		V
EXTBIAS UVLO threshold (rising)	$EXTBIAS\_{RISING}$			4.68		V
EXTBIAS UVLO threshold (falling)	$EXTBIAS\_{FALLING}$			4.42		V
EXTBIAS current Limit	$I_{EXTBIAS}$			110		mA
Driver						
TG1, TG2 Gate Driver On-Resistance	R_{TG_PULLUP}	Gate Pull-Up, V_{BST} – V_{SW} = 5V		2		Ω
	R_{TG_PULLDN}	Gate Pull-Down, V_{BST} – V_{SW} = 5V		1		Ω
BG1, BG2 Gate Driver On-Resistance	R_{BG_PULLUP}	Gate Pull-Up, V_{BST} – V_{SW} = 5V		2		
	R_{BG_PULLDN}	Gate Pull-Down, V_{BST} – V_{SW} = 5V		1		Ω
TG1, TG2, TOFF(MIN)		RT = 90k		200		ns

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 35V, V_{OUT} = 24V, F_{sw} = 300 kHz, T_J = -40°C to +125°C, unless otherwise noted.

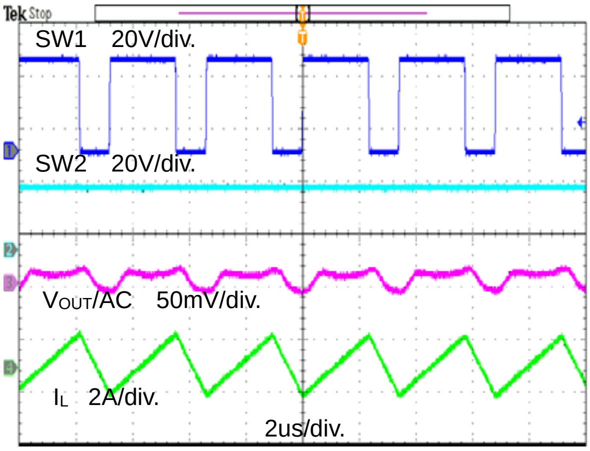


Figure 1. Steady State I_{OUT}=0A CCM

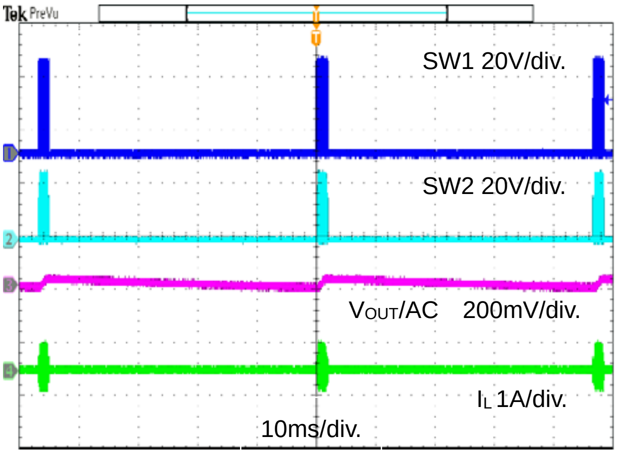


Figure 2. Steady State I_{OUT}=0A DEM

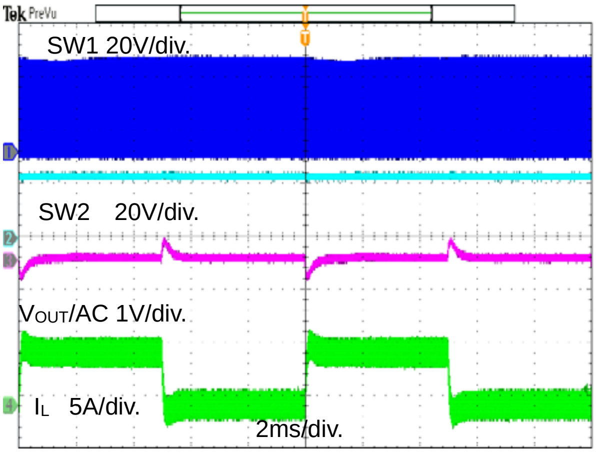


Figure 3. Dynamic Load I_{OUT}=0-5A CCM

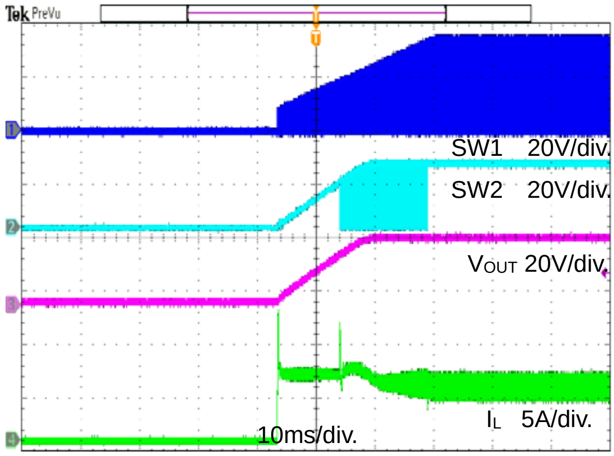


Figure 4. Start Up I_{OUT}=5A CCM

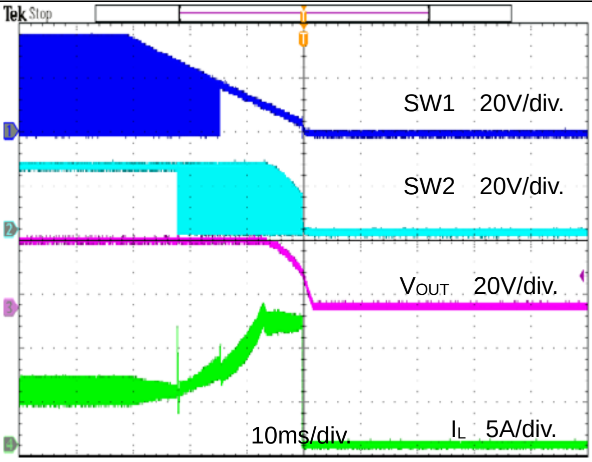


Figure 5. Shut Down Through VIN I_{OUT}=5A

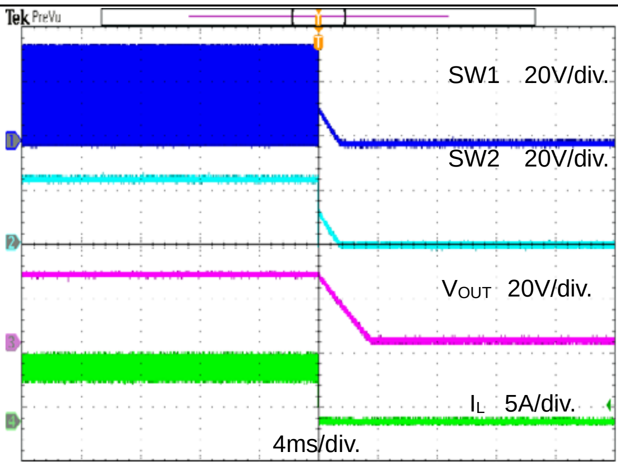


Figure 6. Shut Down Through EN I_{OUT}=5A

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 15V, V_{OUT} = 24V, F_{sw} = 300 kHz, T_J = -40°C to +125°C, unless otherwise noted.

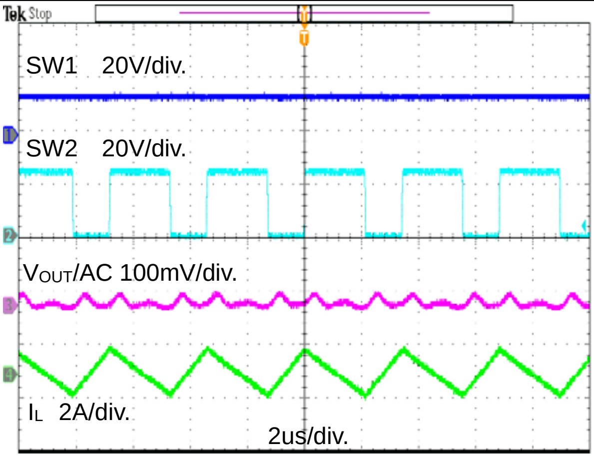


Figure 7. Steady State I_{OUT}=0A CCM

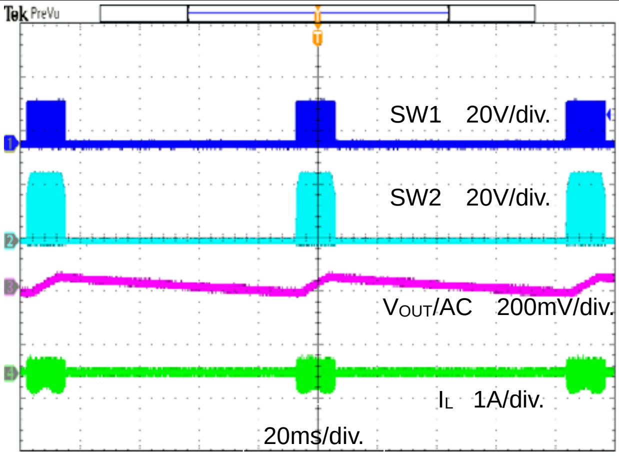


Figure 8. Steady State I_{OUT}=0A DEM

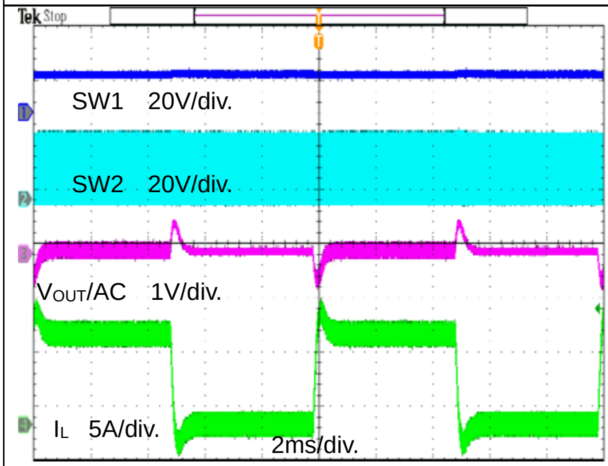


Figure 9. Dynamic Load I_{OUT}=0-5A CCM

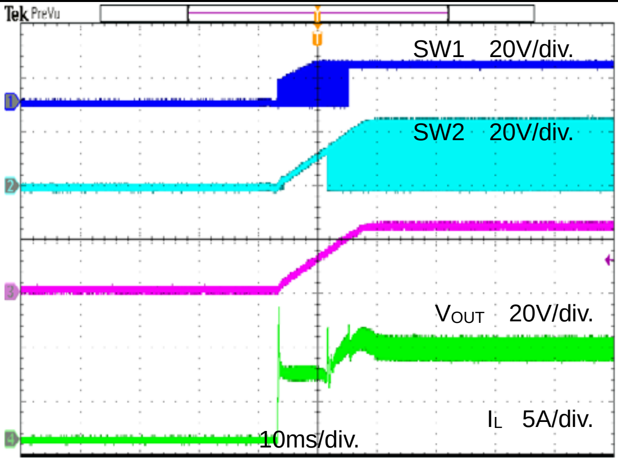


Figure 10. Start Up I_{OUT}=5A CCM

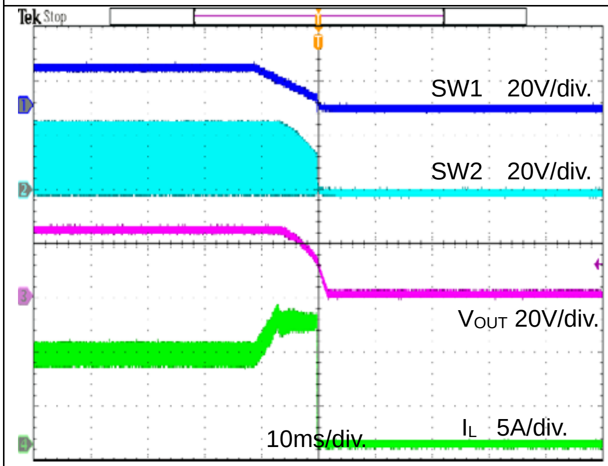


Figure 11. Shut Down Through VIN I_{OUT}=5A

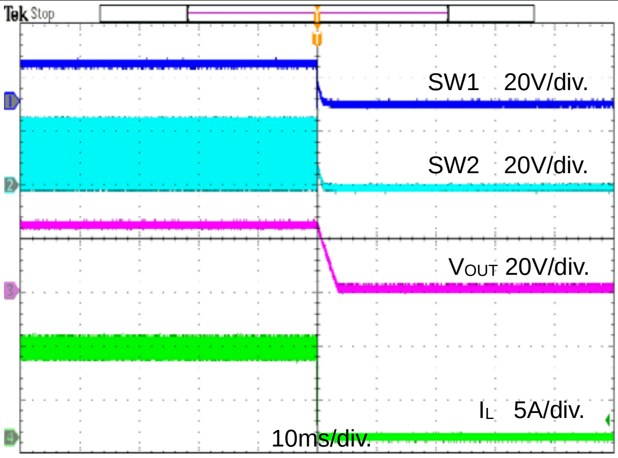


Figure 12. Shut Down Through EN I_{OUT}=5A

TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 24V, V_{OUT} = 24V, F_{sw} = 300 kHz, T_J = -40°C to +125°C, unless otherwise noted.

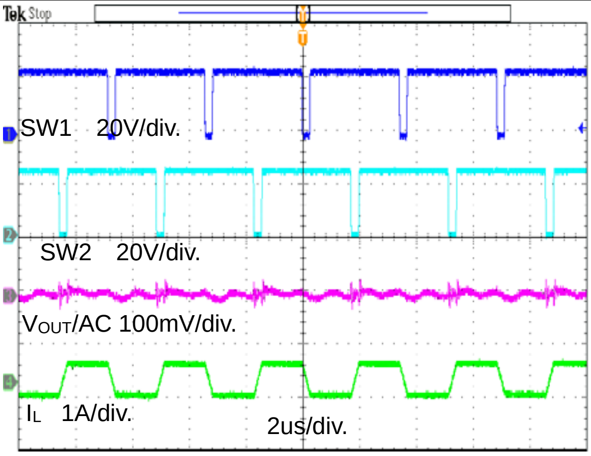


Figure 13. Steady State I_{OUT}=0A CCM

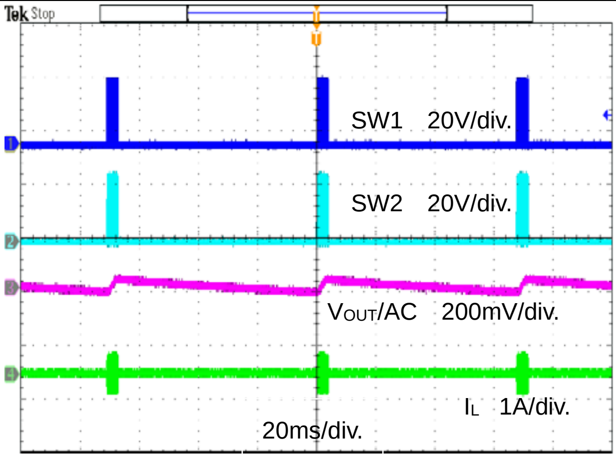


Figure 14. Steady State I_{OUT}=0A DEM

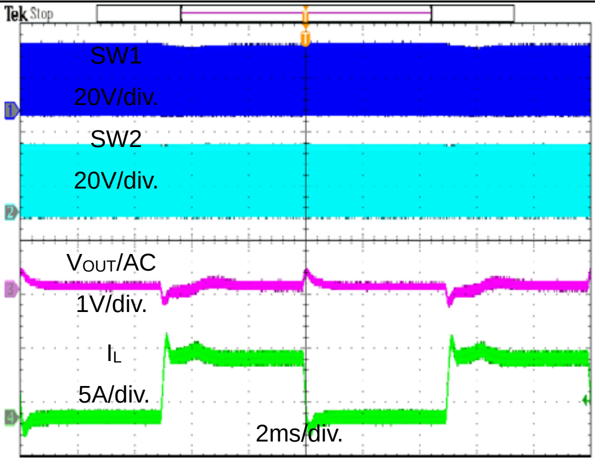


Figure 15. Dynamic Load I_{OUT}=0-5A CCM

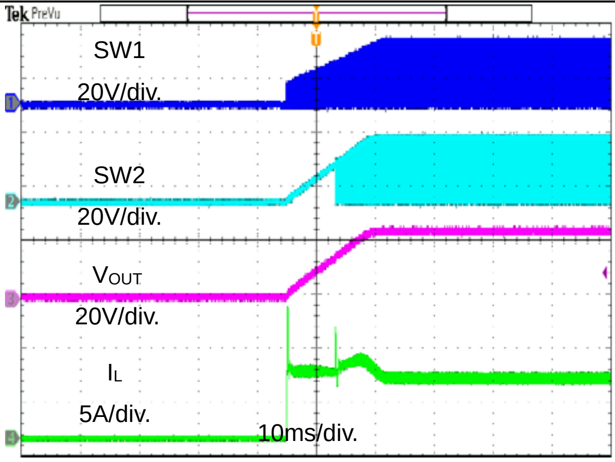


Figure 16. Start Up I_{OUT}=5A CCM

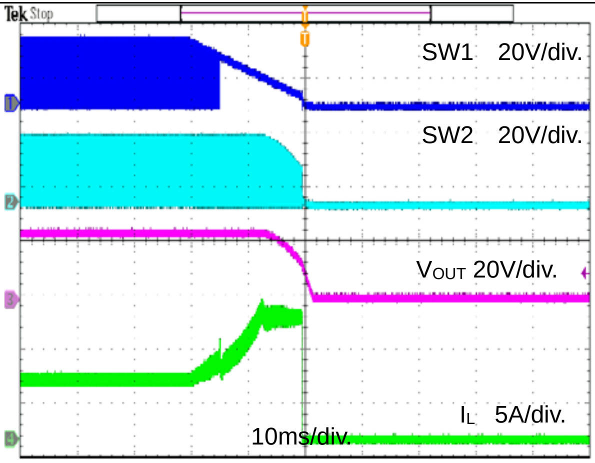


Figure 17. Shut Down Through VIN I_{OUT}=5A

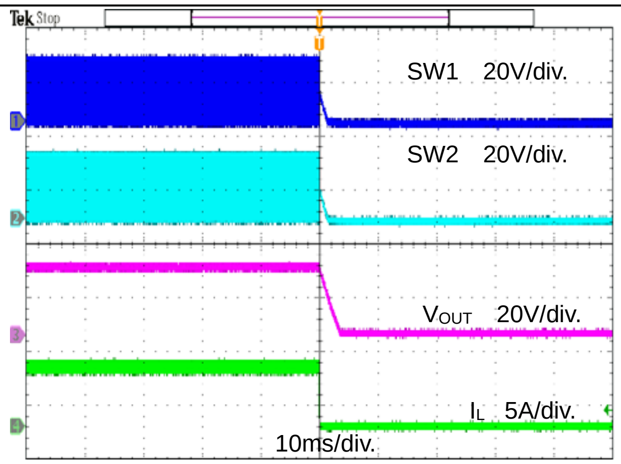


Figure 18. Shut Down Through EN I_{OUT}=5A

FUNCTION DESCRIPTION

Operation

The VE8624 is a current mode 4-switch buck-boost controller that provides an output voltage above, equal to or below the input voltage. The VE8624 uses current mode in buck or boost operation. It operates in buck mode when VIN is greater than VOUT and in boost mode when VIN is less than VOUT. It operates buck-boost mode when VIN is close to VOUT.

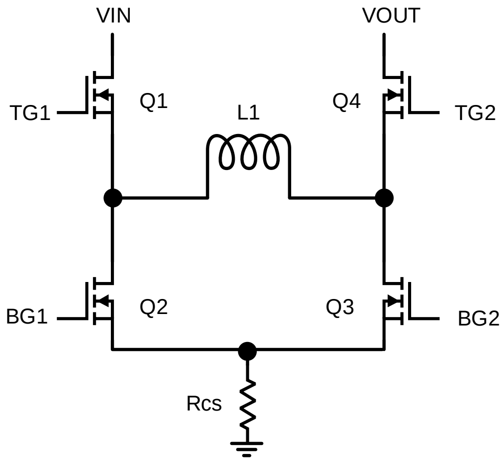


Figure 19. Buck-Boost Controller mode

Boost Mode

In boost mode switch Q1 is always on and switch Q2 is always off. It operates peak current mode boost as Figure 20, behaving likes a typical synchronous boost regulator.

At the start of every cycle, switch Q3 is turned on first. Inductor current is sensed by Rcs when Q3 is turned on. After the sensed current exceeds the reference voltage, which is proportional to COMP, synchronous switch Q3 is turned off and switch Q4 is turned on for the remainder of the cycle.

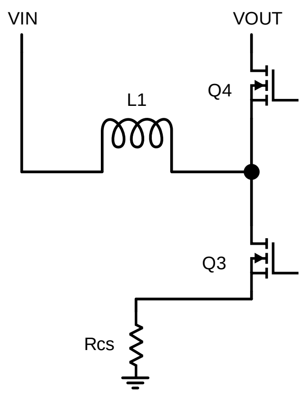


Figure 20. Boost Controller Mode

Buck Mode

In buck mode switch Q4 is always on and switch Q3 is always off. It operates valley current mode buck as Figure 21, behaving likes a typical synchronous buck regulator.

At the start of every cycle, synchronous switch Q2 is turned on first. Inductor current is sensed by Rcs when Q2 is turned on. After the sensed current falls below the reference voltage, which is proportional to COMP, synchronous switch Q2 is turned off and switch Q1 is turned on for the remainder of the cycle.

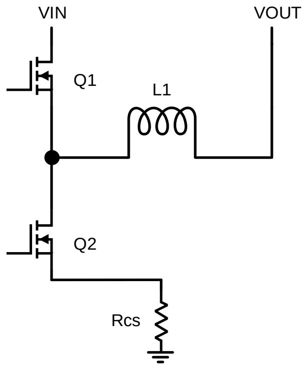


Figure 21. Buck Controller Mode

Buck-boost Mode

When VIN is higher than VOUT but close to VOUT,

The VE8624 enters the buck-boost mode when the duty cycle of buck D_{BUCK} is greater than

D_{bb1} =(T-250ns)/T

Where T is the switching period.

D_{BUCK}=Ton_$_{TG1}$/T

It exits from buck-boost mode and return to buck mode when D_{BUCK} is less than

D_{bb2}=1-(0.25T+200ns)/T

When VIN is lower than VOUT but close to VOUT,

The VE8624 enters the buck-boost mode when the duty cycle of boost D_{BOOST} is less than

D_{bb3} = 250ns/T

Where T is the switching period.

D_{BOOST}=Ton_$_{BG2}$/T

It exits from buck-boost mode and return to boost mode when D_{BOOST} is higher than

D_{bb4} =(0.25T+200ns)/T.

Figure22. shows operating mode vs duty cycle

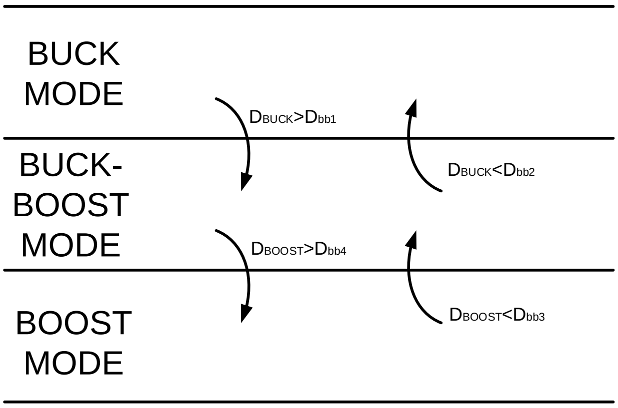


Figure 22. Mode vs Duty Cycle

EN_UVLO

The VE8624 has a dedicated enable (EN_UVLO) control that uses a bandgap - generated precision threshold of 1.2V. By pulling EN_UVLO high or low, the IC can be enabled or disabled.

VCC Regulator Connection

VCC can be powered from both VIN and EXTBIAS. If connecting EXTBIAS to an external power supply, EXTBIAS should be higher than 4.7V but less than 24V. When V_{IN} is less than 5.5V, EXTBIAS should be biased by external source. If V_{OUT} is higher than 5V but less than 24V, EXTBIAS can be connected to V_{OUT} with a resistor or diode. The recommend value of this resistor is 10Ω.

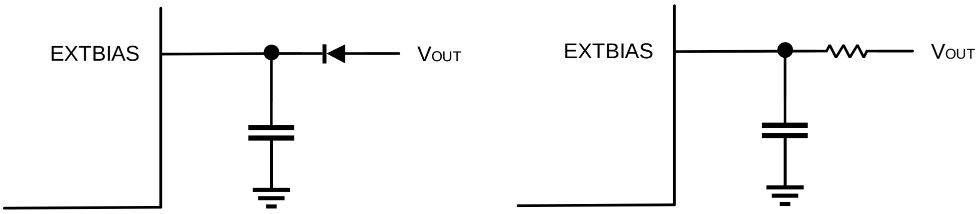


Figure 23. VCC Regulator Connection

Low Current Operation

The VE8624 is recommended to run in forced continuous conduction mode at heavy load by pulling the CCM pin higher than 1.5V. In this mode the controller behaves as a continuous current mode synchronous switching regulator.

However, reverse inductor current from the output to the input is not desired for certain applications. For these applications, the CCM pin must be connected to GND. It also can be pulled low by the C/10 pin when the output current is low. In this mode, switch Q4 turns off when the inductor current flows negative. The Typical Application on the front page is a basic VE8624 application circuit. External component selection is driven by the load requirement, and begins with the selection of R_{SENSE} and the inductor value.

Programming Frequency

The RT frequency adjust pin allows the user to program the switching frequency from 100kHz to 700kHz to optimize efficiency/performance or external component size. Higher frequency operation yields smaller component size but increases switching losses and gate driving current, and may not allow sufficiently high or low duty cycle operation. Lower frequency operation gives better performance at the cost of larger external component size. An external resistor from the RT pin to GND is required; do not leave this pin open.

The Value of RT can be calculated with Equation (1):

$$R_{RT}(K\Omega) = \frac{1000}{0.0202 \times Fsw(KHz)} - 9 \quad (1)$$

Frequency Synchronization

The VE8624 switching frequency can be synchronized to an external clock using the SYNC pin. Driving SYNC with a pulse the duty cycle between 10% and 90%. The frequency of external clock must be higher than 70% of the frequency set by RT.

Soft Start (SS)

Soft start (SS) is implemented to prevent the converter output voltage from overshooting during start-up. When the chip starts up, the internal circuitry generates a soft-start voltage that ramps up from 0V to 3V. When it is lower than REF, SS overrides REF, so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

An external capacitor connected from SS to SGND is charged from an internal 4μA current source, producing a ramped voltage. The soft - start time (T_{SS}) is set by the external SS capacitor and can be calculated by Equation (2):

$$T_{SS}(ms) = \frac{C_{SS}(nF) \times V_{REF}(V)}{I_{SS}(uA)} \qquad (2)$$

Where C_{SS} is the external SS capacitor, V_{REF} is the internal reference voltage (1.2V), and I_{SS} is the 4μA SS charge current.

C/10 Pin

The VE8624 provides an open-drain status pin, C/10, which pulls low when the voltage V_{ISMON} is less than 100mV. For battery charger applications with output current sense and limit, the C/10 provides a C/10 charge termination flag.

Gate Driver

The low-side gate driver is supplied from VCC. The high-side gate driver is supplied from BST. A boot capacitor connected from the BST to the SW provides power to the high-side MOSFET driver. This floating driver has its own under-voltage lockout (UVLO) protection. This UVLO's rising threshold is 3.6V with a hysteresis of 100mV. If the BST voltage is lower than the bootstrap UVLO, the VE8624 enters boot refresh mode to ensure that the BST capacitor is high enough to drive the HS-FET.

ISMON

The ISMON pin provides a linear indication of the current flowing through the output. The equation for V_{ISMON} is

$$V_{ISMON} = 20 \times V_{(ISP-ISN)} \qquad (3)$$

This pin is suitable for driving an ADC input, however, the output impedance of this pin is 80kΩ so care must be taken not to load this pin.

Current control

The CTRL can be used to adjust the current. When the CTRL voltage is less than 1.1V, the voltage on the ISMON pin is limited to the voltage on the CTRL pin.

When the CTRL pin voltage is between 1.1V and 1.4V the voltage on the ISMON pin varies with V_{CTRL}. when V_{CTRL} > 1.4V the voltage on the ISMON pin no longer varies.

Low side current sense

The SNSP and SNSN pins sense the low side current which is used to implement the current mode control and peak valley current limit.

To prevent false triggering due to the switching noise, an RC filter maybe required.

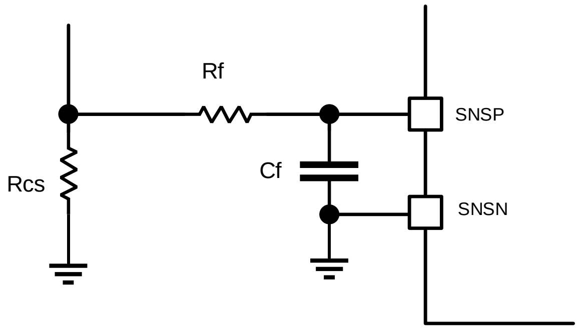


Figure 24. Sensing Configuration

Voltage Loop Compensation

The compensation resistor and capacitor at COMP are set to optimize the voltage loop. The typical value of the compensation capacitor is 22n and the value of compensation resistor is 10k. Higher capacitance and lower resistance will improve stability but will slow the loop response.

Current Loop Compensation

The filter of current sense will improve the stability of current loop. Connecting a RC filter to ISN if the ripple current on the current sense resistor is large. Do not connect the resistor to ISP pin.

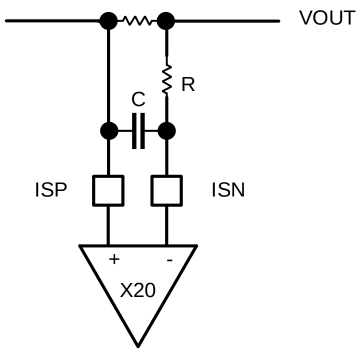


Figure 25. Current Loop Compensation

Another way to filter the current signal is connecting a capacitor to ISMON.

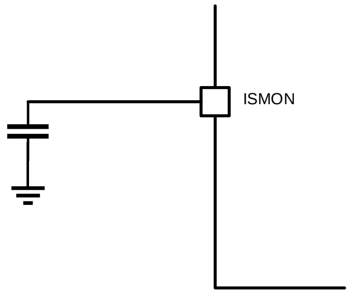


Figure 26. ISMON Configuration

PCB Layout Guidelines

1. The PGND ground plane layer should not have any traces and it should be as close as possible to the layer with power MOSFETs.
2. Place CIN, switch Q1, switch Q2 in one compact area. Place COUT, switch Q3, switch Q4 in one compact area.

3. Keep the high dv/dt SW1, SW2, BST1, BST2, TG1 and TG2 nodes away from sensitive small-signal nodes.
4. The path formed by switch Q1, switch Q2, and the C_{IN} capacitor should have short leads and PC trace lengths. The path formed by switch Q3, switch Q4, and the C_{OUT} capacitor also should have short leads and PC trace lengths.
5. Connect the top driver bootstrap capacitor, C1, closely to the BST1 and SW1 pins. Connect the top driver bootstrap capacitor, C2, closely to the BST2 and SW2 pins.
6. Connect the input capacitors, C_{IN}, and output capacitors, C_{OUT}, closely to the power MOSFETs. These capacitors carry the MOSFET AC current in boost and buck operation.
7. Route SNSN and SNSP leads together with minimum PC trace spacing. Avoid sense lines pass through noisy areas, such as switch nodes. Ensure accurate current sensing with Kelvin connections at the SENSE resistor.
8. Connect the COMP pin compensation network close to the IC, between COMP and the signal ground pins. The capacitor helps to filter the effects of PCB noise and output voltage ripple voltage from the compensation loop.
9. Connect the VCC bypass capacitor close to the IC, between the VCC and the power ground pins. This capacitor carries the MOSFET drivers' current peaks.

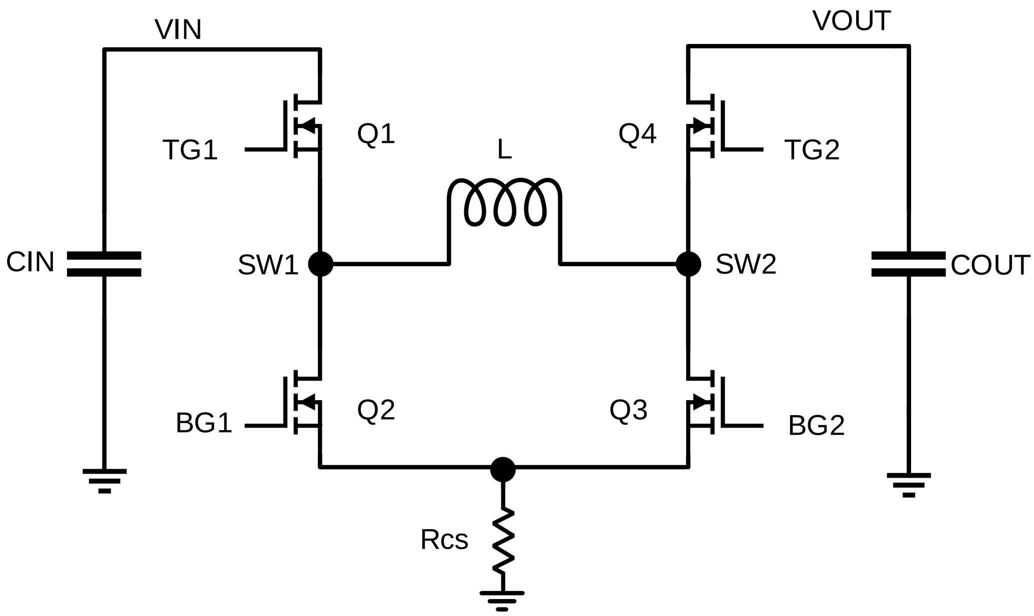
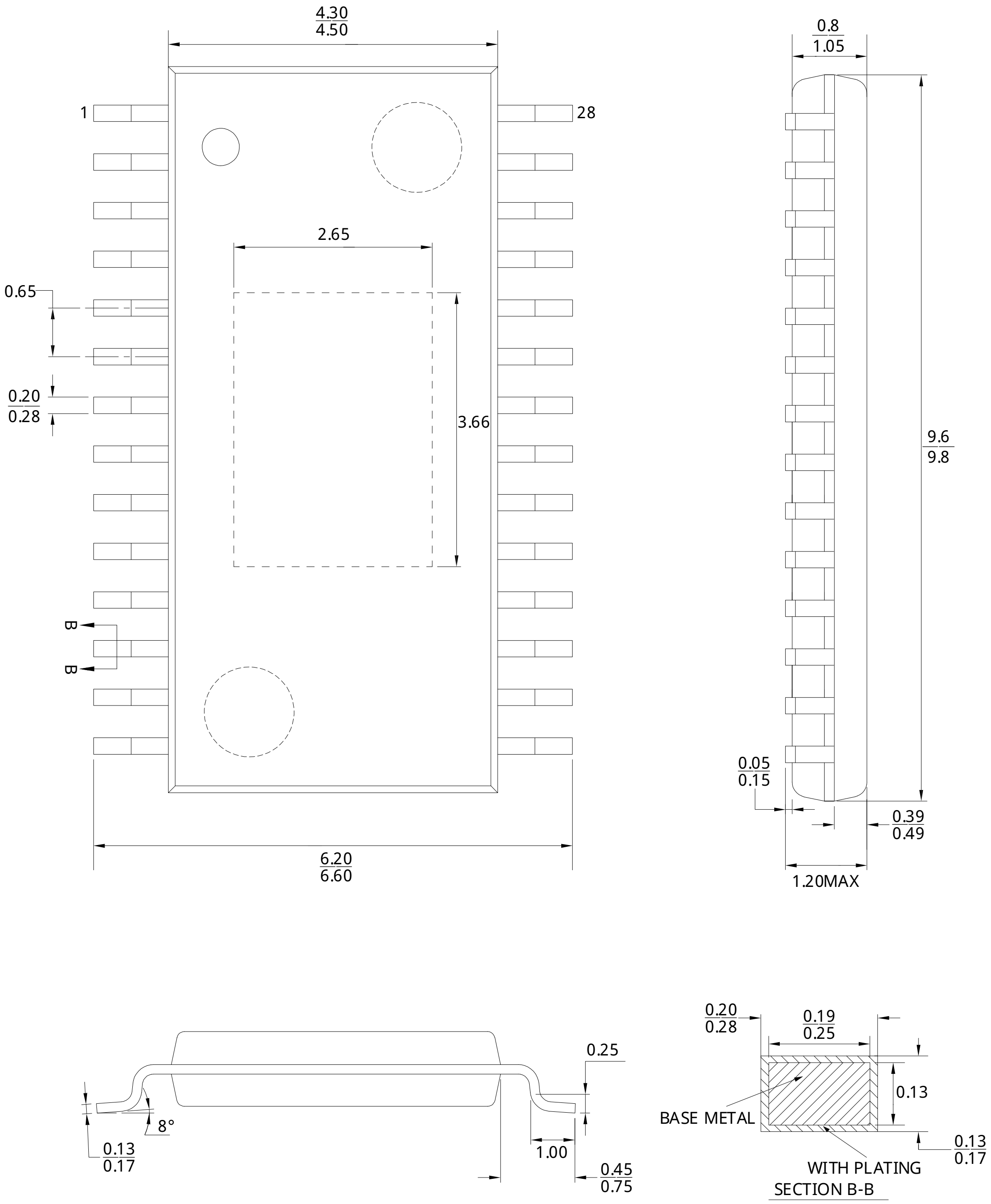


Figure 27. Power Stage of Buck-Boost

PACKAGE INFORMATION

TSSOP28-EP



REVISION HISTORY

Revision	Data	Description
1.0	2024-10-15	Initial Release

NOTICE: The information in this document is subject to change without notice. Users should warrant and guarantee that third party Intellectual Property rights are not infringed upon when integrating Volturrent products into any application. Volturrent cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Volturrent product. Volturrent will not assume any legal responsibility for any said applications.