High-Speed Inductive Sin/Cos Output Position Sensor Chip

1. Features

- AEC-Q100 Grade0 automotive grade qualified
- Compliant with ISO26262 Functional Safety ASIL-B
- Supports maximum rotational speed exceeding 600K rpm
- Accuracy ≤±0.36°el, maximum ≤0.05°
- Supports Auto-Calibration Function
- Programmable via Single-Wire Interface through Power Pin or Programming Pin
- Diagnostic functions: open circuit, short circuit, overvoltage, overtemperature，overcurrent，coil Input open-circuit
- High-reliability design: 48V voltage tolerance for power and output pins
- Strong anti-electromagnetic interference capability
- Suitable for compact through-shaft mounting configuration
- Operating temperature range: -40℃ to 150℃
- Package type: Small TSSOP-16、QFN3*3-16

2. Applications

- Main drive motor
- Robotic joint control
- EPS motor
- Electronic Brake Booster
- High-Speed Absolute Rotary Position Encoder

3. Description

The SC60410 is a series of non-contact, high-speed, high-precision inductive position sensor ICs designed for high-speed absolute position sensing in automotive and industrial applications. Based on the eddy-current effect principle, the device accurately measures target position by detecting changes in induced voltage caused by the displacement of a metallic target over a set of coils.

The SC60410 allows fine-tuning of the output signal via the programming pin after self-calibration. It supports a maximum speed exceeding 600K rpm under a single-cycle coil design and achieves ultra-low transmission delay (<4 μs), with near-zero delay characteristics during steady-state motor operation.

The SC60410 processes captured signals through filtering, amplification, demodulation, and offset compensation, providing differential sine and cosine outputs. The encoder sensor achieves an accuracy of ≤0.36° el per electrical cycle.

The SC60410 is available in 16-pin TSSOP-16 and QFN3*3-16 packages, featuring matte tin plating and halogen-free green molding compound to meet environmental requirements.

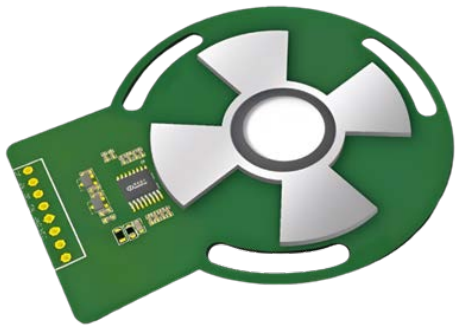

Fig.1 Schematic diagram of the work

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4. Pin Description

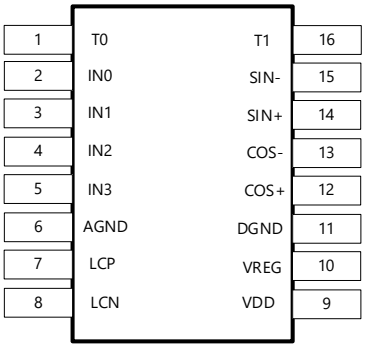


Fig.2 TSSOP16 Pin Description

Pin		Type	Pin function description
Name	No.		
T0	1	Output	Test Pin
IN0	2	Input	Receiver Coil Input 0
IN1	3	Input	Receiver Coil Input 1
IN2	4	Input	Receiver Coil Input 2
IN3	5	Input	Receiver Coil Input 3
AGND	6	GND	Analog Ground
LCP	7	Input	Excitation Coil Output Positive
LCN	8	Input	Excitation Coil Output Negative
VDD	9	Power	Power Supply
VREG	10	Output	Output of the Internal High-Voltage LDO, Requires an External 100 nF Decoupling Capacitor
DGND	11	GND	Digital GND
COS+	12	I/O	Analog: Cosine Signal Positive Output
COS-	13	I/O	Analog: Cosine Signal Negative Output
SIN+	14	I/O	Analog: sine Signal Positive Output
SIN-	15	Output	Analog: sine Signal Negative Output
T1	16	I/O	Single-Wire Programming Pin

16-Pin QFN 3X3 Package
(Top View)

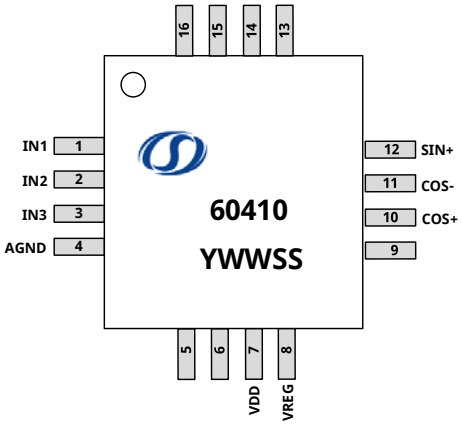


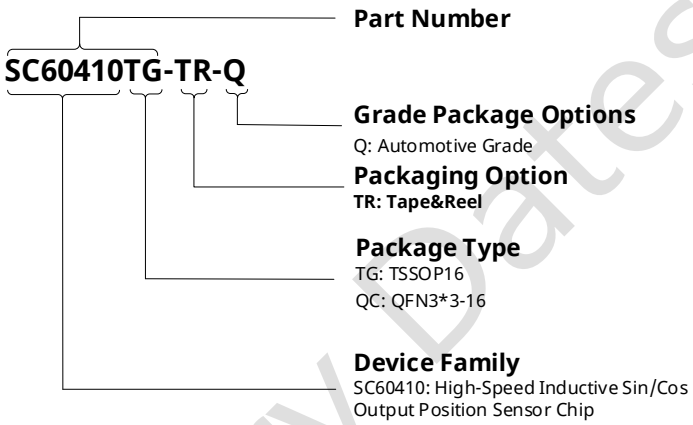
Fig.3 QFN3*3-16 Pin Description

Pin		Type	Description
Name	No.		
IN1	1	Input	Receiver Coil Input 1
IN2	2	Input	Receiver Coil Input 2
IN3	3	Input	Receiver Coil Input 3
AGND	4	GND	Analog GND
LCP	5	Input	Excitation Coil Output Positive
LCN	6	Input	Excitation Coil Output Negative
VDD	7	Power	Power Supply
VREG	8	Output	Output of the Internal High-Voltage LDO, Requires an External 100 nF Decoupling Capacitor
DGND	9	Gnd	Digital GND
COS+	10	Output	Analog: Cosine Signal Positive Output
COS-	11	Output	Analog: Cosine Signal Negative Output
SIN+	12	Output	Analog: Sine Signal Positive Output
SIN-	13	Output	Analog: Sine Signal Negative Output
T1	14	I/O	Single-Wire Programming Pin
T0	15	I/O	Test Pin
IN0	16	Input	Receiver Coil Input 0

5. Ordering Information

Ordering Information	Mark	Output	Ambient(℃)	Package	Pack	Amount
SC60410TG-TR-Q	60410	±SIN/COS	-40~150	TSSOP16	Tape&Reel	3000Pcs/Reel
SC60410QC-TR-Q	60410	±SIN/COS	-40~150	QFN3*3-16	Tape&Reel	5000Pcs/Reel

Ordering Information Format



6. Absolute Maximum Ratings

Over Full Operating Temperature Range (Unless Otherwise Specified) (1)

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{DD}	Supply voltage withstand	t<60s	-5.5	48	V
V_{REG}	Regulator voltage withstand	t<60s	-0.3	5.5	V
V_{IO}	Output voltage withstand		-12	24	V
$V_{LCP/LCN}$	Excitation coil input		-0.5	5.5	V
V_{INX}	Receiver coil input		-0.5	5.5	V
SDA	Digital I/O (Input/Output)		-0.5	5.5	V
SCL	Digital clock input		-0.5	5.5	V
T_A	Operating temperature		-40	150	℃
T_J	Maximum junction temperature		-55	165	℃
T_{STG}	Storage temperature		-65	175	℃

Note:

(1)Stresses above those listed here may cause permanent damage to the device. Prolonged exposure to absolute maximum ratings may affect the reliability of the device.

7. ESD Protection

Symbol	Parameter	Test Conditions	Min.	Max.	Unit
V_{ESD_HBM}	HBM	Human failure model, refer to ANSI/ESDA/JEDEC-001 standard	-4	4	kV
V_{ESD_CDM}	CDM	Device failure model, refer to ANSI/ESDA/JEDEC-002 standard	-750	750	V

8. Operating Characteristics

Condition: unless otherwise specified, V_{DD} = 5V ±10%, T_A = -40°C to 150°C [1]

Symbol	Parameter	Test Condition	Min.	Typ.[1]	Max.	Unit
Power Supply Characteristics						
V_{DD_5v}	5V Application operating voltage	Refer to 5V application circuit connection	4.5	5.0	5.5	V
$V_{DD\_3.3v}$	3.3V Application operating voltage	Refer to 3.3V application circuit connection	3.0	3.3	3.6	V
I_{DD_5V}	5V Application operating voltage	V_{DD}=5.0V	-	8.0	12	mA
$I_{DD\_3.3V}$	3.3V Application operating voltage	V_{DD}=3.3V	-	7.0	11	mA
V_{VREG}	5V Application operating current	V_{DD}=5.0V	4.5	4.8	-	V
C_{VREG}	3.3V Application operating current		47	100	470	nF
V_{OVP}	5V Operation, VREG pin voltage	Outputs disabled when supply voltage exceeds this threshold	6.5	7.0	7.5	V
V_{OVP_HYS}	VREG pin decoupling capacitor		0.2	0.5	0.8	V
V_{UVR}	Overvoltage detection threshold	Outputs disabled when supply voltage falls below this	3.4	3.7	4.3	V
V_{UVR_HYS}	Overvoltage detection hysteresis		0.1	0.3	0.5	V
LC oscillator characteristics						
I_{OSC}	LC oscillator drive current	L=3μH，C=1nF，Rs=2Ω	2.0	-	10	mA
V_{OSC}	LC oscillator oscillation amplitude	L=3μH，C=1nF，Rs=2Ω	3.0	3.5	4.0	Vpp
F_{OSC}	LC oscillator oscillation frequency	L=3μH，C=1nF，Rs=2Ω	2	4	5	MHz
L_{OSC}	Excitation coil inductance		2	-	10	μH
Coil input signals						
V_{PPIN}	IN_X input signal amplitude		5	-	100	mV
SIN/COS Analog Outputs						
V_{PP5V}	5V application SIN/COS output amplitude	V_{DD}=5.0V	1	2	3.8	Vpp
$V_{PP3.3V}$	3.3V application SIN/COS output amplitude	V_{DD}=3.3V	1	1.25	2.64	Vpp

V_{DC}	SIN/COS DC level		-	2.5	-	V
OFF_{VPP}	SIN/COS output amplitude deviation		-8	0.0	8	mV
OFF_{VDC}	SIN/COS DC level deviation		-5	0.0	5	mV
R_{LOAD}	SIN/COS pull-up/downresistance		4.7	47	100	kΩ
C_{LOAD}	SIN/COS output load capacitance	Output port capacitive load	4.7	10	47	nF
T_{DELAY}	Sine/Cosine Output Signal Delay	Constant Rotation at 1000 RPM	-	-	4	μs
Noise	Output Noise	Maximum Gain, No Output Filter, Coil Input Shorted	-	2	5	mV
Rpm	Rotation Speed	Single-Cycle Coil	-	-	600000	rpm

Operating Characteristics (Continued)

Symbol	Parameter	Test Conditions	Min.	Typ.(1)	Max.	Unit
A/D Conversion Characteristics						
$R_{ES(SD)}$	ADC resolution		-	14	-	Bit
$T_{(ON)}$	Startup time		-	-	5	ms
Diagnostic Function						
Dsat_lo	Active Diagnostic Output Level	Pull-Down Resistor R≥4.7kΩ	-	0.5	1	%VDD
		Pull-Up Resistor R≥4.7kΩ	99	99.5	-	%VDD
$BV_{SS}PD$	Passive Diagnostic Output Level (Open-Circuit)	VSS Open-Circuit, Pull-Down Resistor, 4.7kΩ≤R≤47kΩ	-	0	3	%VDD
$BV_{SS}PU$		VSS Open-Circuit, Pull-Up Resistor, 4.7kΩ≤R≤47kΩ	97	98	-	%VDD
$BV_{DD}PD$		VDD Open-Circuit, Pull-Down, 4.7kΩ≤R≤47kΩ	-	0	1	%VDD
$BV_{DD}PU$		VDD Open-Circuit, Pull-Up, 4.7kΩ≤R≤47kΩ	96.5	98	-	%VDD
OTP	Overtemperature Protection		-	175	-	℃
$I_{\_OCP}$	Overcurrent Protection		-		30	mA

Note：

(1) Values are typical at ambient temperature +25°C and VDD = 5V.

9. Functional Module

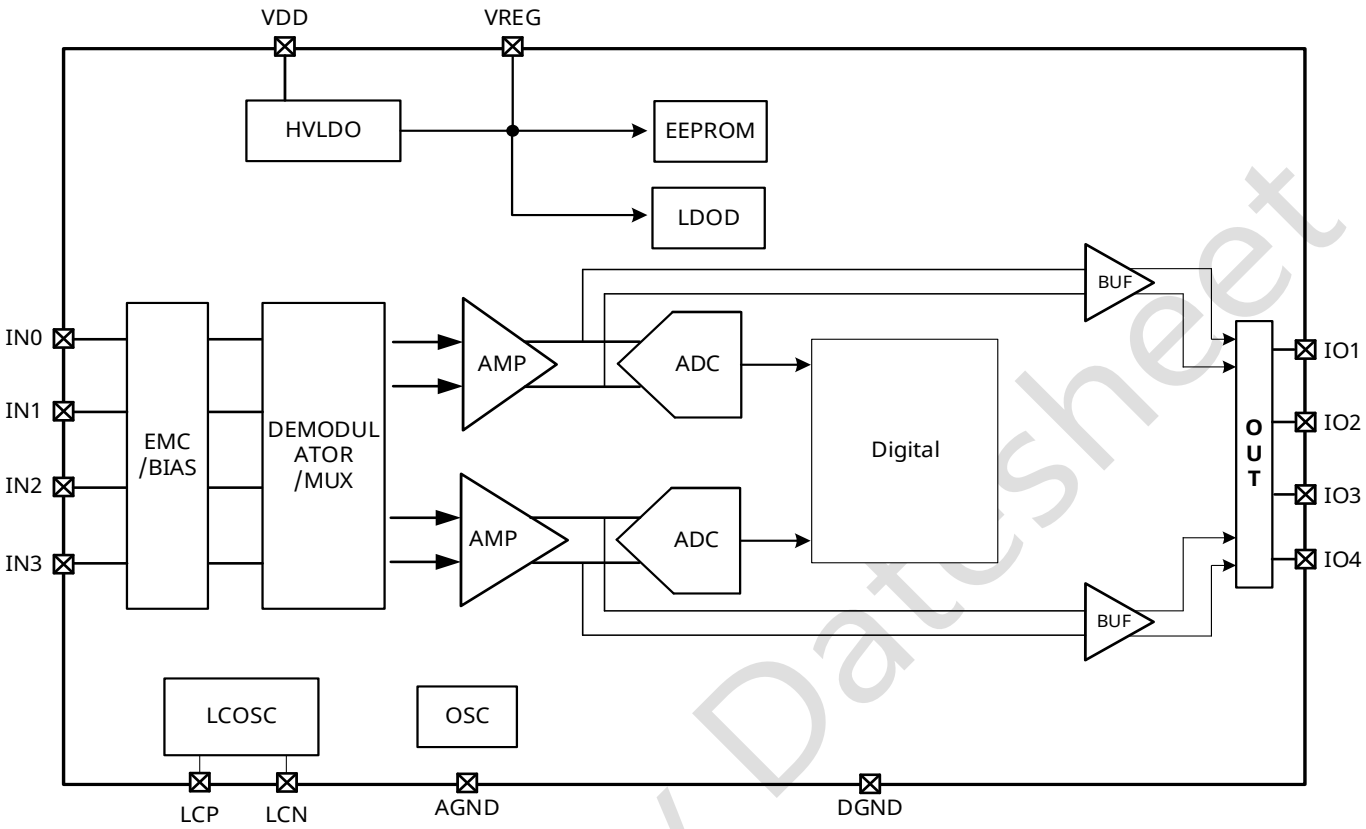


Fig.4 Functional Block Diagram

10. Functional Description

10.1. Auto-Calibration

External Trigger:

1、With the external rotor in uniform rotation at a speed ≤ 600K rpm (Rotation speed affects auto-calibration completion time. For 1 kHz, the completion time is 2 s);

2、After power-on, the device internally detects the voltage on output pins within 500 μs. When the output pins OUT1~OUT4 correspond to the status pattern '1001' (SIN+ and COS- connected to supply via 47 kΩ, SIN- and COS+ connected to ground via 47 kΩ), the auto-calibration mode is triggered;

3、Internally processes the received signals, identifying the peak-to-peak amplitude and common-mode deviation after ADC conversion;

4、By comparing with target values, internal feedback adjusts the signal gain and VOS compensation to bring the received signals within the target threshold range;

5、Auto-calibration completes when both signal channels are within the target threshold range. The current gain and VOS compensation values are automatically programmed into the EEPROM, and a completion flag is issued, resulting in an additional 10 mA of device current consumption;

6、If the internal gain or VOS compensation reaches its limit before the received signals are adjusted within the target threshold range, the optimal values are programmed into the EEPROM, and a completion flag is issued, resulting in an additional 10 mA of device current consumption. (The extra current is disabled after a power reset and does not affect normal operation. The 10 mA indicates that auto-calibration has completed. To determine whether auto-calibration was successful, query the status of the dedicated internal register via communication);

Active Programming Trigger:

1、After device power-on, initiate active programming by sending the designated code to enter auto-calibration mode;

Steps 2 through 6 are identical to those for external trigger operation.

10.2. Diagnostic Function

1、Power Management

VDD incorporates overvoltage and reverse-polarity protection, continuously monitors for undervoltage or overvoltage conditions, and also provides overcurrent protection.

2、Coil Input Diagnostics

Continuously monitors coil inputs for open-circuit condition.

3、Wire-Break Diagnostics

Continuously monitors power and ground lines for open-wire conditions.

4、Temperature Diagnostics

Continuously monitors internal die temperature; outputs are disabled when the preset threshold is exceeded.

11. EEPROM Description

11.1. EEPROM List

Page	Row	bit7	bit6	bit5	bit4	bit3	bit2	bit1	bit0
0	0	EE_CODE<3>	PWMMS	CAL_LSEL<3:0>				EE_CODE<2>	CalibMASK
	1	PID_FILTER_SEL<1:0>		DP<13:8>					
	2	DP<7:0>							
	3	TRIMBG<2:0>			TRIMOSC<4:0>				
	4	GAIN_TH<1:0>		VOS_TH<1:0>		VOSEN	LC_AMSEL	LC_IREF	G1
	5	EE_CODE<1>	CRCMASK	OTPMASK	OVPMASK	UVLOMASK	RXDMASK	LCFREMASK	LCVPPMASK
	6	ABZEDG<1:0>		ABZ_HYS<1:0>		ABZWID<1:0>		ABZLINE<2:1>	
	7	ABZLINE<0>	PWMCTRL	PWMPOL	PWMT	EE_CODE<0>	DIR	OUTMOD<1:0>	
	8	VOS3_SIN<3:0>				VOS3_COS<3:0>			
	9	G2<3:0>				G3<3:0>			
	A	V3P3EN	G2F_SIN<2:0>			CLK_SLOW	G2F_COS<2:0>		
	B	VOS_SIN_G<7:0>							
	C	VOS_COS_G<7:0>							
	D	VOS_SIN_F<7:0>							
	E	VOS_COS_F<7:0>							
	F	CRC							

11.2. Register Bit Description

Symbol	Bit	R/W	Bit Address	Description
EE_CODE[3:0]	4	R/W	0x00[7]+0x00[1]+0x05[7]+0x07[3]	EEPROM erase/write operations are enabled when EE_CODE = 4'b1100
CalibMASK	1	R/W	0x00[0]	Auto-Calibration and Auto-Zeroing Functions Disabled 0: Enabled 1: Disabled
CAL_LSEL[3:0]	4	R/W	0x00[5:2]	Auto-Calibration Max/Min Counting Duration 6: Applicable frequency 60 Hz (auto-calibration completion time: 10 s)
PID_FILTER_SEL<1:0>	2	R/W	0x01[7:6]	Rotation Speed Selection 00: 600k RPM 11: 60k RPM
GAIN_TH<1:0>	2	R/W	0x04[7]+0x04[6]	Device Auto-Calibration VPP Threshold 0x04[7]=0: Coarse Adjustment ±15% 0x04[7]=1: Coarse Adjustment ±10% 0x04[6]=0: Fine Adjustment ≤1.5% 0x04[6]=1: Fine Adjustment ≤1%
VOS_TH<1:0>	2	R/W	0x04[5]+0x04[4]	Device Auto-Calibration VOS Threshold 0x04[5]=0: Coarse Adjustment ±2‰ 0x04[5]=1: Coarse Adjustment ±1‰ 0x04[4]=0: Fine Adjustment ≤2‰ 0x04[4]=1: Fine Adjustment ≤1‰
VOSEN	1	R/W	0x04[3]	Internal VOS Enable 0: VOS Disabled 1: VOS Enabled
LC_AMSEL	1	R/W	0x04[2]	LC Output VPP Selection 0: 2.8V 1: 3.8V
G1	1	R/W	0x04[0]	First-Stage Gain Selection 0: ×2 1: ×4
CRCMASK	1	R/W	0x05[6]	CRC Diagnostics Disable 0: Enabled 1: Disabled
OTPMASK	1	R/W	0x05[5]	OTP Diagnostics Disable 0: Enabled 1: Disabled
OVPMASK	1	R/W	0x05[4]	OVP Diagnostics Disable 0: Enabled 1: Disabled
UVLOMASK	1	R/W	0x05[3]	UVLO Diagnostics Disable 0: Enabled 1: Disabled
RXDMASK	1	R/W	0x05[2]	RX_OPEN Diagnostics Disable 0: Enabled 1: Disabled
LCFREMASK	1	R/W	0x05[1]	LC Frequency Diagnostics Disable 0: Enabled 1: Disabled
LCVPPMASK	1	R/W	0x05[0]	LC Amplitude Diagnostics Disable 0: Enabled 1: Disabled
OUTMOD	2	R/W	0x07[1:0]	Output Mode Configuration 2: Analog Sine/Cosine Output Mode
VOS3_SIN<3:0>	4	R/W	0x08[7:4]	SIN Channel Third-Stage VOS Compensation
VOS3_COS<3:0>	4	R/W	0x08[3:0]	COS Channel Third-Stage VOS Compensation
G2<3:0>	4	R/W	0x09[7:4]	Second-Stage Gain Adjustment: 8–123 ×1.2
G3<3:0>	4	R/W	0x09[3:0]	Third-Stage Gain Adjustment: 1–4 ×1.1
V3P3EN	1	R/W	0x0A[7]	3.3V Application Flag
G2F_SIN<2:0>	3	R/W	0x0A[6:4]	SIN Channel Gain Fine Tuning

EEPROM Explanation of Table Sequence

G2F_COS<2:0>	3	R/W	0x0A[2:0]	COS Channel Gain Fine Tuning
VOS_SIN_G<7:0>	8	R/W	0x0B[7:0]	SIN Channel VOS Compensation, Coarse Adjustment
VOS_COS_G<7:0>	8	R/W	0x0C[7:0]	COS Channel VOS Compensation, Coarse Adjustment
VOS_SIN_F<7:0>	8	R/W	0x0D[7:0]	SIN Channel VOS Compensation, Fine Adjustment
VOS_COS_F<7:0>	8	R/W	0x0E[7:0]	COS Channel VOS Compensation, Fine Adjustment
CRC	8	R	0x0F[7:0]	CRC

12. SIN/COS Analog Output

Typical application diagram

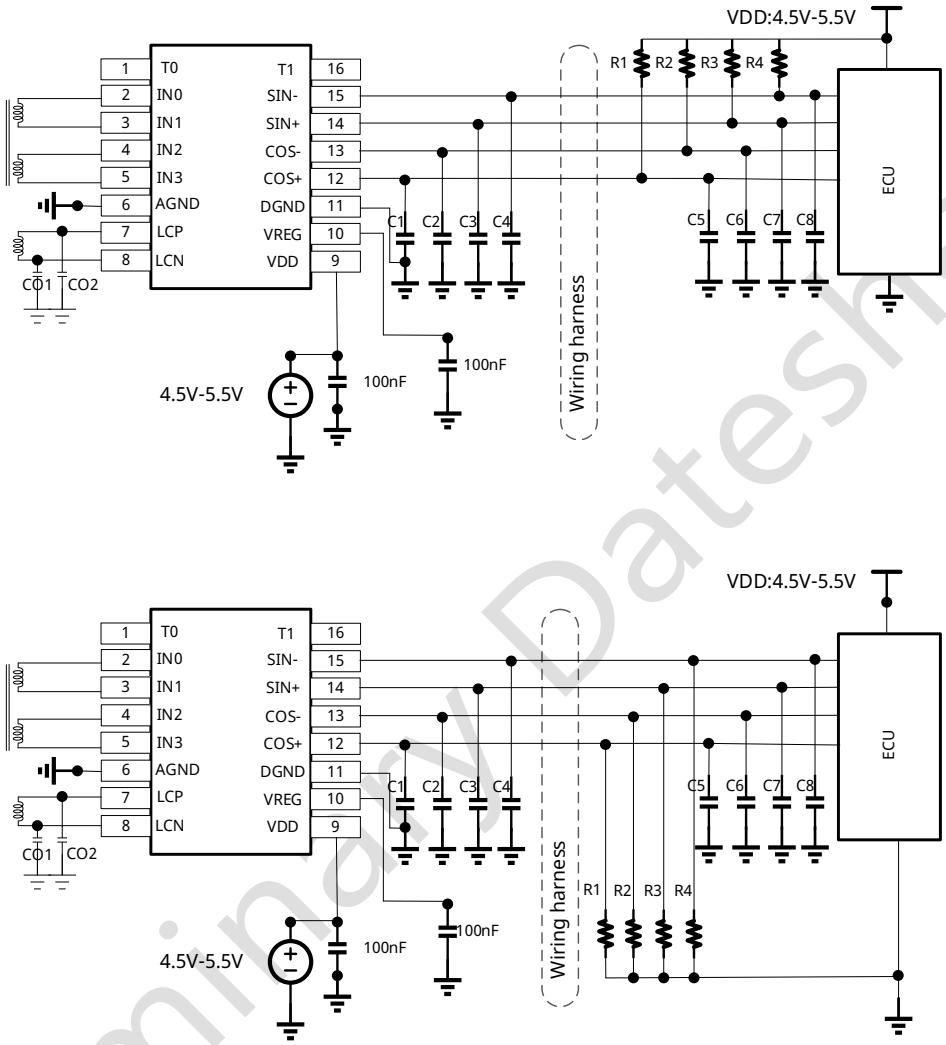


Fig.5 Analog output application diagram(The circuit before the dashed line represents the sensor section, while the circuit after the dashed line corresponds to the ECU side)

Note：

(1) Output Capacitance Range: 4.7 nF to 47 nF

(2) Excitation Capacitance is calculated as follows：

$$Fosc = \frac{1}{2\pi.\sqrt{\frac{CO1.CO2.Losc}{CO1+CO2}}}$$

The acceptable range for Fosc is 1.5 MHz to 5 MHz. Select the appropriate capacitance based on the PCB excitation coil inductance Losc, typically within the range of 300 pF to 2 nF.

SIN/COS output waveform diagram

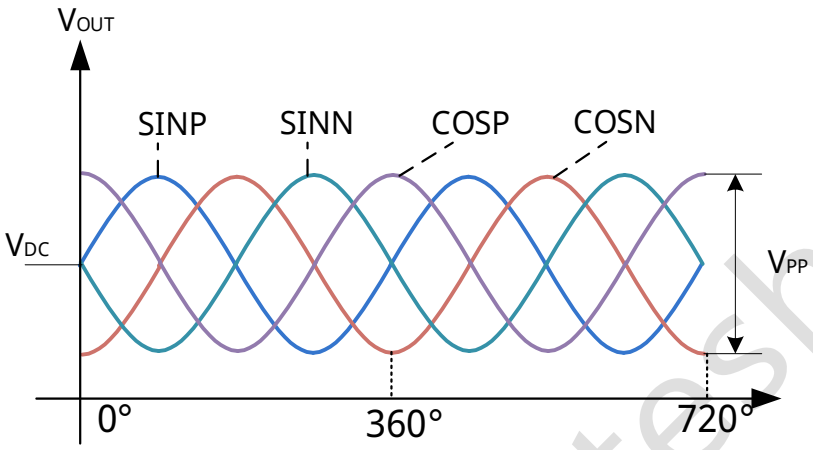


Fig.6 Analog output waveform diagram

13. Power Supply Connection Configuration

5V Application Circuit Connection

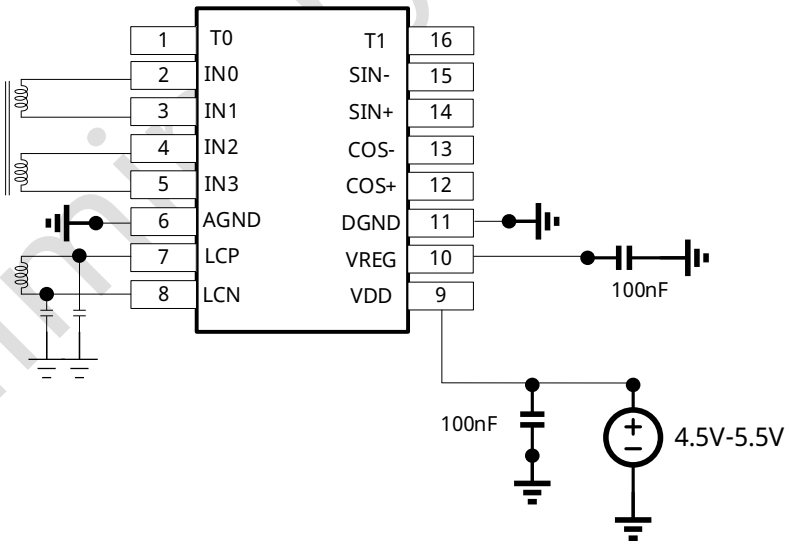


Fig.7 5V Power supply circuit diagram

3.3V Application Circuit Connection

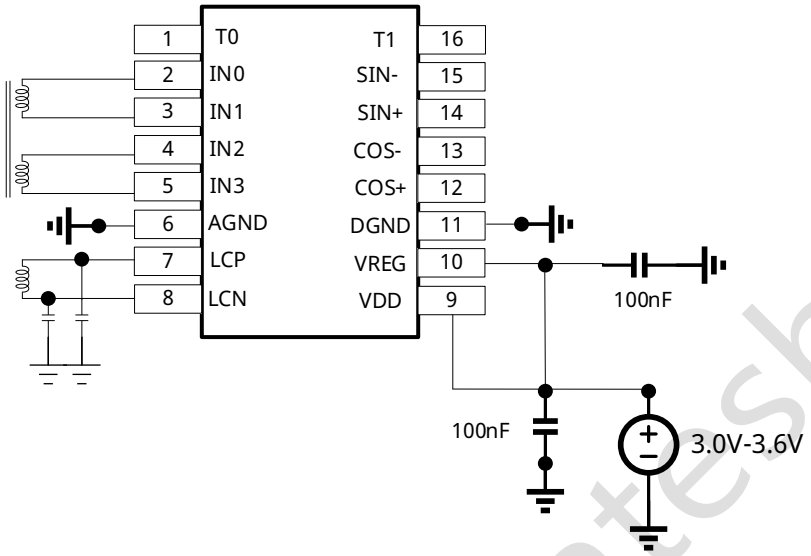
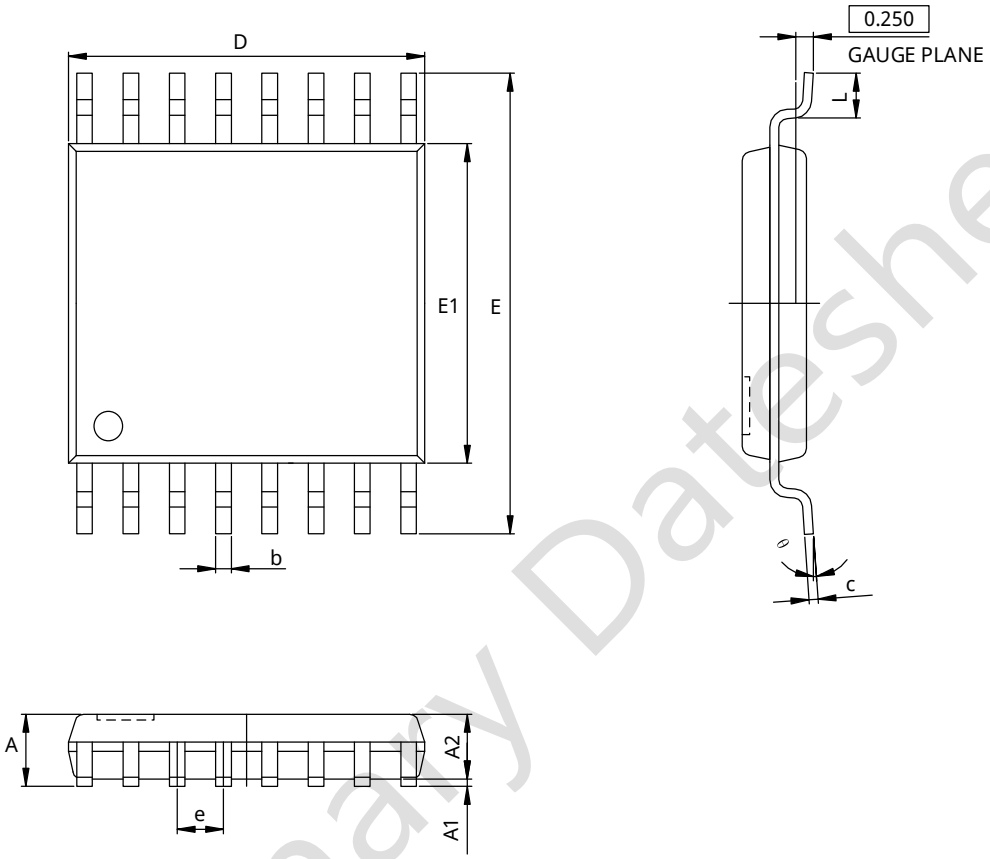


Fig.8 3.3V Power circuit diagram

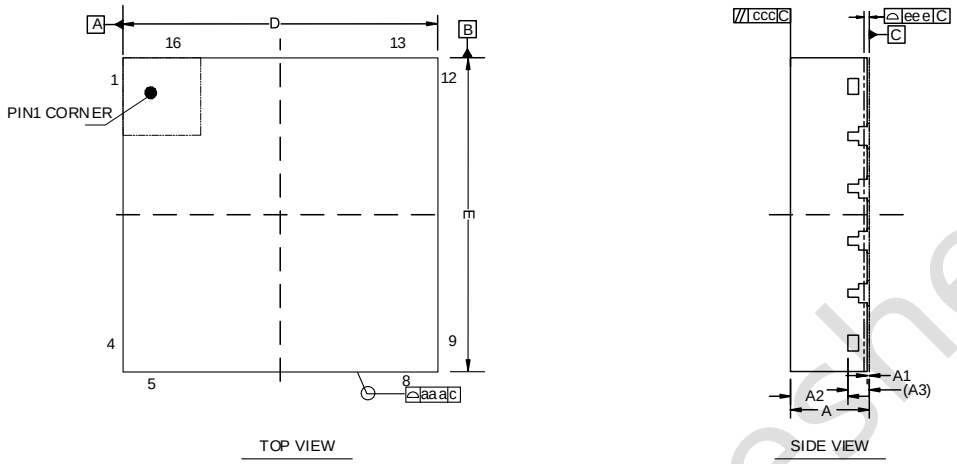
14. Package Information

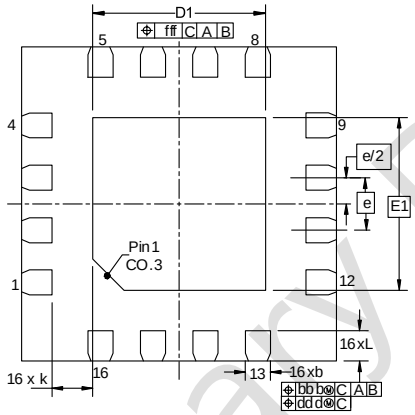
14.1. TSSOP16 Package (TG)



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	-	1.200	-	0.047
A1	0.050	0.150	0.002	0.006
A2	0.800	1.000	0.031	0.039
b	0.190	0.300	0.007	0.012
c	0.090	0.200	0.004	0.008
D	4.900	5.100	0.193	0.201
E	6.250	6.550	0.252(BSC)	
E1	4.300	4.500	0.169	0.177
e	0.650(BSC)		0.026(BSC)	
L	0.500	0.700	0.020	0.028
θ	1°	7°	1°	7°

14.2. QFN3*3-16 Package (QC)



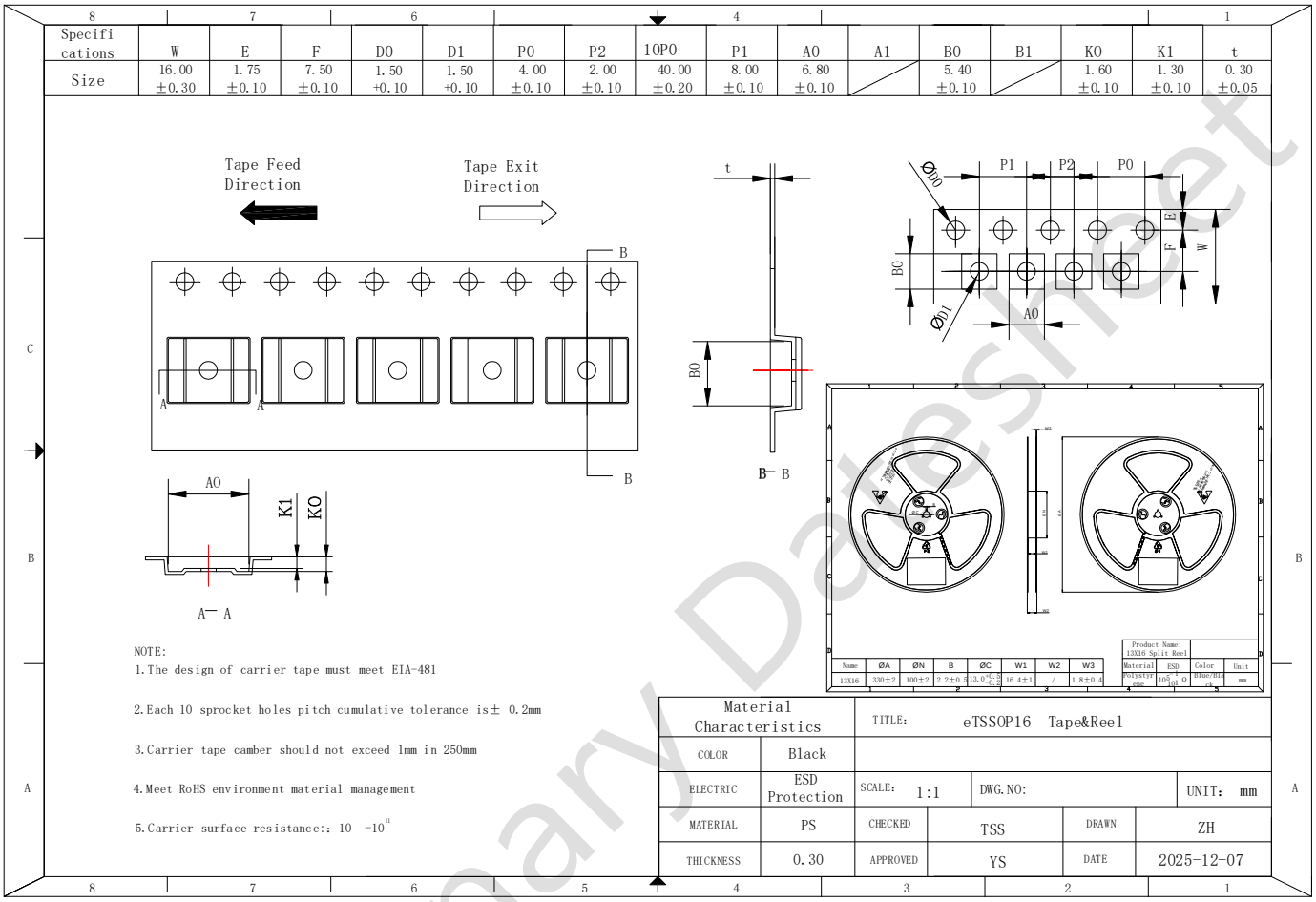


		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.70	0.75	0.80
STAND OFF		A1	0.00	0.02	0.05
MOLD THICKNESS		A2	---	0.55	---
L/F THICKNESS		A3	0.203 REF		
BODY SIZE	X	D	3.00 BSC		
	Y	E	3.00 BSC		
EP SIZE	X	D1	1.50	1.65	1.80
	Y	E1	1.50	1.65	1.80
LEAD WIDTH		b	0.18	0.24	0.30
LEAD PITCH		e	0.500 BSC		
LEAD TIP TO EXPOSED PAD EDGE		k	0.385 BSC		
LEAD LENGTH		L	0.19	0.29	0.39
PACKAGE EDGE TOLERANCE		aaa	0.1000		
MOLD FLATNESS		ccc	0.1000		
COPLANARITY		eee	0.0800		
LEAD OFFSET		bbb	0.1000		
		ddd	0.0500		
EXPOSED PAD OFFSET		fff	0.1000		

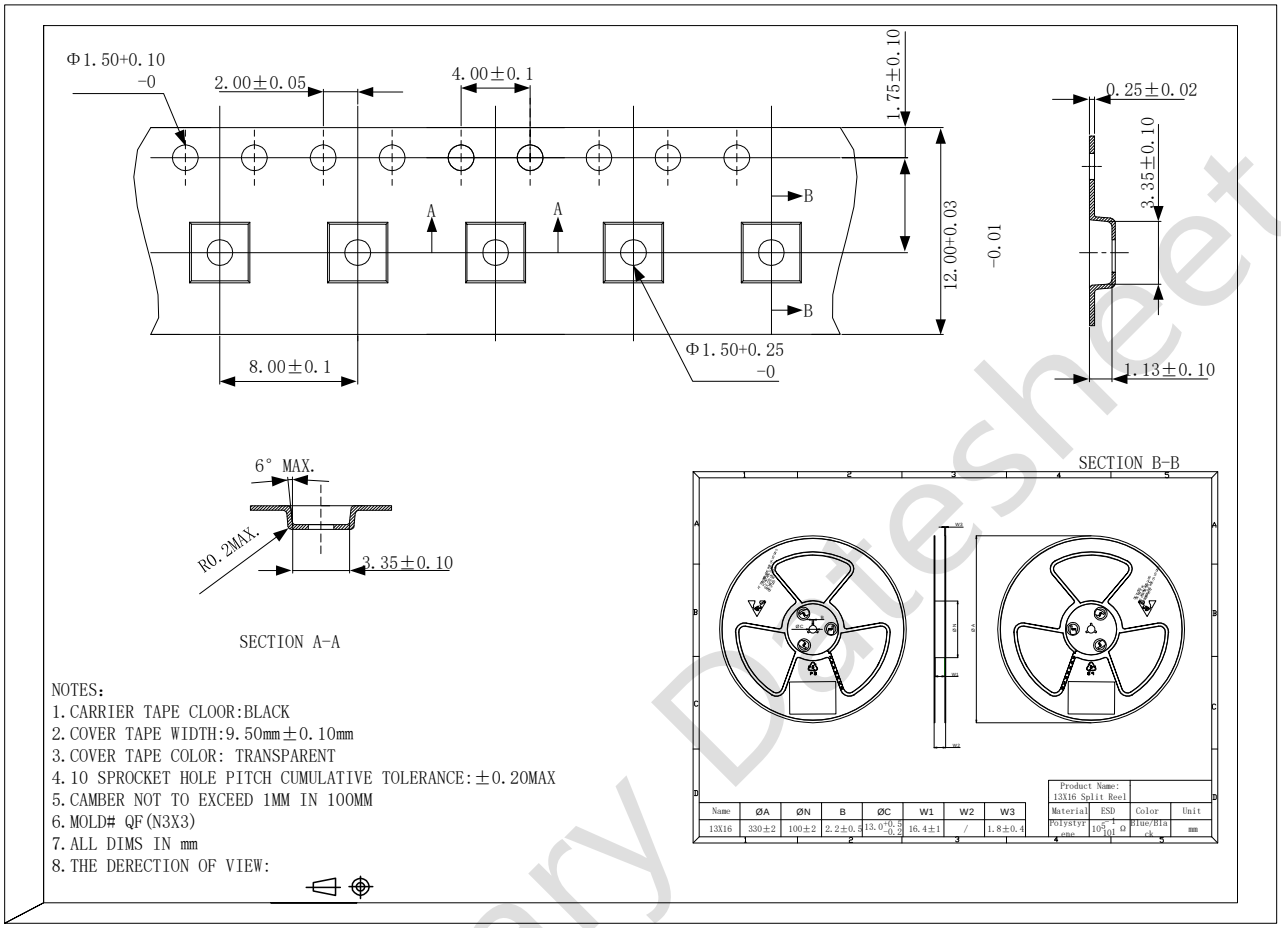
15. Package Specification

15.1. TSSOP16 Package (TG)

Specifications	W	E	F	D0	D1	P0	P2	10P0	P1	A0	A1	B0	B1	K0	K1	t
Size	16.00 ±0.30	1.75 ±0.10	7.50 ±0.10	1.50 +0.10	1.50 +0.10	4.00 ±0.10	2.00 ±0.10	40.00 ±0.20	8.00 ±0.10	6.80 ±0.10		5.40 ±0.10		1.60 ±0.10	1.30 ±0.10	0.30 ±0.05



15.2. QFN3*3 Package (QC)



16. Revision History

Revision	Date	Description
Rev.V0.1	2025-12-10	Preliminary datasheet
Rev.V0.2	2026-01-11	Add the packing information
Rev.V0.3	2026-01-28	Update output-pin define